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Filing Date: January 15, 2004 Art Unit: not yet assigned

Serial No. ~~not yet assigned~~ ^{10/758 802} Examiner: not yet assigned

For: METHODS OF FABRICATING A SEMICONDUCTOR DEVICE HAVING
MULTI-GATE INSULATION LAYERS AND SEMICONDUCTOR DEVICES
FABRICATED THEREBY

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
<u>MEW</u>		US 6,222,225 B1	4/24/2001	Nakamura, et al.		

Examiner: Matthew E. Warner

Date Considered: 3/13/05